REMARKS

Claims 1-19, 26-32, and 43 are pending. Claims 1-19, 26-32, and 43 are rejected. No amendments have been made to the Claims or the Specification. No new matter has been added.

103 Rejections

Claims 1-5, 10-14, and 43 are rejected under 35 USC 103(a) as being obvious over Lloyd et al. in view of Loewenstein.

The Examiner is respectfully directed to independent Claim 1 which recites that an embodiment of the present invention is directed to a method of timestamping events in a primary event stream, the method comprising:

> receiving the primary event stream;
> apportioning events in the primary event stream among a plurality of secondary event streams;
> and timestamping events in each of the plurality of secondary event streams wherein each timestamp has a first component comprising a specific clock cycle of a reference clock and a second component comprising a time at which the given event occurs within the specific clock cycle.

Claim 10 recites limitations similar to Claim 1. Claims 2-5 depend from Claim 1 and recite further features of the claimed invention. Claims 11-14 and 43 depend from Claim 10 and recite further features of the claimed invention.

The rejection suggests Lloyd et al discloses an event stream distributor coupled to receive the primary event stream, for apportioning events in the primary event stream

across a plurality of secondary event streams. The Applicant respectfully disagrees. The Applicant understands Lloyd et al. to disclose a system for analysis of arrival times between pairs of events, and the analysis of continuous data streams. See col. 1, ln. 6-11. More specifically, Lloyd et al. discloses two systems, one where a data stream representing the separation of a series of events is measured and stored, and the other where the pulse arrival distribution is stored. See col. 6, ln. 24-31. The former case does not call for apportioning events among a plurality of secondary event streams as claimed; rather, Lloyd et al. calls for the output of the system to provide information regarding the timing between successive events. See col. 6, ln. 1-3. The latter case also does not call for apportioning events among a plurality of secondary event streams as claimed; rather, this second case is equated to a correlator, described by Lloyd et al. as providing a record of the "distribution of times separating consecutive events." See col. 2, ln. 9-13.

While Lloyd et al. mention the use of "a number of channels," the Applicant contends that this function is distinctly different from the embodiment of the invention recited in Claim 1 (Claim 10 contains similar limitations) because the channels used in Lloyd et al. do not carry secondary event streams, but are instead used solely as incremental counters, to indicate how often a particular interval of time has elapsed between events in the event stream. However, in contrast to the claimed embodiment, the primary event stream is never apportioned between these channels. Lloyd et al. does not anticipate or render obvious a method of timestamping events which includes apportioning events in the primary event stream among a plurality of secondary event streams. Loewenstein does not remedy this defect of Lloyd et al.

Similarly, Lloyd et al. does not anticipate or render obvious a method for timestamping events in a primary event stream which includes timestamping events in each of the plurality of secondary event streams wherein each timestamp has a first component comprising a specific clock cycle of a reference clock and a second component comprising a time at which the given event occurs within the specific clock cycle. As noted above, the Applicant understands Lloyd et al. to disclose a system for analysis of arrival times between pairs of events; in neither of the disclosed cases does the system disclosed by Lloyd timestamp events, wherein each timestamp has the two components as claimed. Loewenstein does not remedy this defect of Lloyd et al.

The rejection suggests combining the disclosures of Lloyd et al. with the disclosures of Loewenstein. However, these references do not suggest such a combination. Lloyd et al. recites a number of limitations of the systems available prior to the system disclosed, and explains the steps taken to overcome these limitations. More specifically, Lloyd et al. notes two primary considerations in the design of the system disclosed. First, that it operate faster than contemporary real-time electronic correlators would allow, see Col. 2 ln. 32-39, and second, that it not produce the tremendous amount of data that multi-stop or non-stop timing circuits would when used for high resolution analysis, see Col. 1 ln. 64 – Col. 2 ln. 9. There is no suggestion to combine the teachings of Loewenstein with Lloyd et al. as suggested by the rejection because these fundamental restrictions on the system disclosed by Lloyd et al. would have to be discarded. Namely, the system would be necessarily slow, with greater amounts of data manipulation to be

done, and greater amounts of data would necessarily be produced, to allow for the timestamping information to be collected. As such, the combination of Loewenstein with Lloyd et al. would render the system disclosed by Lloyd et al. unsuitable for its intended purpose. Therefore, the Applicant respectfully contends that the combination of Lloyd et al. with Loewenstein et al. is not suggested.

Moreover, even if Lloyd et al. and Loewenstein were combined, Loewenstein does not overcome the deficiencies of Lloyd et al. disclosed above. The Applicant respectfully contends that Loewenstein does not anticipate or render obvious a method for timestamping events in a primary event stream in which the primary event stream is apportioned among a plurality of secondary event streams. The Applicant understands Loewenstein to disclose a time-to-digital converter which derives the time of an event through use of a ramp signal generator. See Col. 5, ln. 16-41. Loewenstein does not disclose apportioning a primary event stream among a plurality of secondary event streams. Consequently, Loewenstein, alone or in combination with Lloyd et al., does not anticipate or render obvious the embodiments of the Applicant's invention as disclosed in Claims 1 and 10.

Therefore, the Applicant respectfully submits that the claimed embodiments of the invention as set forth in Claims 1 and 10 are in condition for allowance. Accordingly, the Applicant also respectfully submits that Claims 2-5 and 43, and 11-14, dependent on Claims 1 and 10 respectively, overcome the Examiner's basis for rejection under 35 U.S.C. 103(a), as they are dependent on allowable base claims.

Claims 6-9 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Lloyd et al., in view of Loewenstein, and in further view of Boerker.

The remarks above concerning Lloyd et al. and Loewenstein, with regard to Claims 1 and 10 are equally applicable to Claims 6-9 and 19.

The rejection suggests combining the disclosures of Boerker with Lloyd et al. However, these two references are do not suggest the combination recited in the Claims. As noted above, Lloyd et al. requires a minimum output of data. Boerker discloses a system where all of the data that comes into the system is preserved; only the transfer rate is reduced. See Fig. 1, elements 18 and 25; see ¶ 60. Applying the disclosures of Boerker would therefore render the system disclosed in Lloyd et al. unsatisfactory for its intended purpose. The Applicant's respectfully contend that Boerker and Lloyd et al. do not suggest the combination disclosed in the Claims, and cannot serve to anticipate or render obvious Claims 6-9 and 19.

Moreover, even if Boerker and Lloyd et al. were combined, Boerker does not overcome the deficiencies of Lloyd et al. and Loewenstein, discussed above. Boerker does not anticipate or render obvious a method for timestamping events in a primary event stream in which the primary event stream is apportioned among a plurality of secondary event streams. The Applicant respectfully asserts that Boerker discloses a data reception circuit for receiving a data stream with a high data transfer rate, see ¶ 55, then separating

such stream into a plurality of slower data streams, see ¶ 57, for the purpose of outputting the same data stream at a lower transfer rate, see ¶ 60. Boerker does not disclose the apportioning of an event stream, nor does it disclose timestamping events in the secondary event streams; the Applicant respectfully contends that the sole purpose of Boerker is to disclose a method of reducing the transfer rate of a data stream. Consequently, Boerker, alone or in combination with Lloyd et al. and/or Loewenstein, does not anticipate or render obvious the embodiments of the Applicant's invention as disclosed by Claims 6-9 and 19.

Therefore, the Applicant respectfully contends that the claimed embodiments of the invention set forth in Claims 6-9 and 19 are in condition for allowance.

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being obvious over Lloyd et al., in view of Loewenstein and in further view of Fransson.

The remarks above concerning Lloyd et al. and Loewenstein with regard to Claims 1 and 10 are equally applicable to Claims 15-18.

Frannson does not overcome the deficiencies of Lloyd et al. and Loewenstein, discussed above. Frannson does not anticipate or render obvious a timestamp system which includes an event stream distributor for apportioning events in the primary event stream across a plurality of secondary event streams. The Applicant understands Fransson to disclose a counting circuit, in which the number of incoming pulses of a clock

signal are counted, see Col. 1, ln. 20-25. More specifically, Frannson purports to disclose a high resolution counting circuit, see Col. 2, ln. 33-54, in which a high frequency clock signal triggers a signal generator, which in turn triggers a plurality of secondary counters, which in turn output to a summing circuit, with the final output of the disclosed system being a counter signal, see Col. 2, ln. 2-37. Frannson does not disclose the apportioning of a primary event stream across a plurality of secondary event streams. Consequently, Frannson, alone or in combination with Lloyd et al. and/or Loewenstein, does not anticipate or render obvious the embodiments of the Applicant's invention disclosed in Claims 15-18.

Therefore, the Applicant respectfully contends that the claimed embodiments of the invention as set forth in Claims 15-18 are in condition for allowance.

Claims 26-32 are rejected under 35 U.S.C. 103(a) as being obvious over Frannson, in view of Tambe et al. The Examiner is respectfully directed to Claim 26, which recites that an embodiment of the invention is a circuit for apportioning events in a signal, comprising:

> a first counter coupled to receive a signal having a plurality of events; and a first plurality of gates, each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter, wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter.

Claims 27-32 depend from Claim 26, and recite further features of the claimed invention.

The rejection notes that Frannson does not disclose "the first counter coupled to receive the signal having a plurality of events and wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter," see pp. 7-8. The Applicant respectfully agrees.

The rejection suggests that Tambe et al. discloses a first counter coupled to receive the signal having a plurality of events and wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter. The Applicant respectfully disagrees. Tambe et al. does not overcome the deficiencies of Frannson detailed above. The Applicant understands Tambe et al. to disclose a system for digital gate generation for a signal measurement system, and more specifically to disclose a method for digitally controlling the gate for a timing counter, see Abstract. The Applicant respectfully contends that Tambe et al. does not disclose a circuit for apportioning events in a signal which includes a first plurality of gates, each gate of the first plurality of gates coupled to receive a respective control signal from the first counter, wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter. The rejection equates the gates discussed in Tambe et al. with the first plurality of gates required by the embodiment of the Applicant's invention disclosed in Claim 26. The gates discussed in Tambe et al., however, cannot be equated with the gates disclosed in Claim 26. Tambe et al. discloses "a signal called a gate" which starts and stops event and time counters, see Col. 1, ln. 22-23; this gate signal, and how to modify it to

overcome certain limitations, is the subject of the system disclosed. Consequently, Tambe et al., alone or in combination with Frannson, does not anticipate or render obvious the embodiment of the Applicant's invention disclosed in Claim 26.

Therefore, the Applicant respectfully submits that the claimed embodiments of the invention as set forth in Claim 26 is in condition for allowance. Accordingly, the Applicant also respectfully submits that Claims 27-32, dependent on Claim 26, overcome the Examiner's basis for rejection under 35 U.S.C. 103(a), as they are dependent on allowable base claims.

Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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